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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/521,280	03/07/2000	Stephan Voges	EFIM0252	9230

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EXAMINER	
KISS, ERIC B	
ART UNIT	**PAPER NUMBER**
2192	

MAIL DATE	DELIVERY MODE
05/31/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/521,280	VOGES ET AL.	
	Examiner	Art Unit	
	Eric B. Kiss	2192	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 May 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,5,57 and 59* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,5,57 and 59* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on May 22, 2007, has been entered.

Claims 1, 5, 57, and 59 are pending.

Response to Amendment

2. Applicant's amendments to the claims do not appropriately address the rejection of claims 1, 5, 57, and 59 under 35 U.S.C. § 112, second paragraph. Accordingly, this rejection is maintained as set forth below.

Response to Arguments

3. Applicant's arguments filed May 22, 2007, have been fully considered but they are not persuasive.

Regarding the instant application, the trademark VERILOG is used to describe particular simulation environment, i.e., simulating VERILOG code. If the trademark or trade name is used in a claim as a limitation to identify or describe a particular material or product, the claim does not comply with the requirements of the 35 U.S.C. 112, second paragraph. *Ex parte Simpson*, 218 USPQ 1020 (Bd. App. 1982); MPEP § 2173.05(u). The claim scope is uncertain since the trademark or trade name cannot be used properly to identify any particular material or product. MPEP § 2173.05(u). In fact, the value of a trademark would be lost to the extent that it became

descriptive of a product, rather than used as an identification of a source or origin of a product. *Id.* Thus, the use of a trademark or trade name in a claim to identify or describe a material or product would not only render a claim indefinite, but would also constitute an improper use of the trademark or trade name. *Id.*

LoCicero discloses a "single executable program" (see, e.g., "Simulation executable" in Figure 1 on p. 7) adapted to create "a primary thread running VERILOG code on a simulator that runs VERILOG code" ("Each segment of . . . converted Verilog that constitutes a coroutine . . . is allocated a separate thread . . . ." LoCicero at 6,) and "a secondary thread" running an interpreter that interprets a scripted routine comprising a user-defined call that is mapped to a VERILOG task ("Each segment of C++, encapsulated C . . . is allocated a separate thread . . . ." LoCicero at 6; See also LoCicero at 7 (Interfaces to the three Verilog constructs to conditionally suspend execution are also provided for the user's pure C++ code); LoCicero at 11 ("To create this cosimulation engine in as natural an environment as possible, C++ was extended with much of the functionality of Verilog . . . .")).

Again, the examiner asserts that the internal conversion of VERILOG code does not change the fact that the LoCicero system simulates VERILOG code. The VERILOG to C++ parser is merely one tool used within the VERILOG simulator disclosed by LoCicero to implement the simulation of VERILOG code. VERILOG code goes in, and simulation results come out. *E.g.*, *LoCicero*, Figure 1. The input to the LoCicero system is VERILOG source code, and the converted code, "simulates identically to the original Verilog source code." *LoCicero* at p. 6. The resulting typical simulation, "is composed of Verilog gates and `always` blocks, and C++ objects." *Id.* Further, LoCicero discloses, "Each segment of C++, encapsulated

C, or converted Verilog that constitutes a coroutine . . . is allocated a separate thread so that the operating system can support its execution concurrent with the other coroutines." *Id.* at pp. 6-7. It is clear from the disclosure of LoCicero that VERILOG code is inputted into the system and simulated, along with all of its VERILOG-specific functionality, and thus, the simulation engine of LoCicero may be considered a simulator that runs VERILOG code.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1, 5, 57, and 59 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1, 5, 57, and 59 contain the trademark/trade name VERILOG. Where a trademark or trade name is used in a claim as a limitation to identify or describe a particular material or product, the claim does not comply with the requirements of 35 U.S.C. 112, second paragraph. See *Ex parte Simpson*, 218 USPQ 1020 (Bd. App. 1982). The claim scope is uncertain since the trademark or trade name cannot be used properly to identify any particular material or product. A trademark or trade name is used to identify a source of goods, and not the goods themselves. Thus, a trademark or trade name does not identify or describe the goods associated with the trademark or trade name. In the present case, the trademark/trade name is used to identify/describe a particular simulation environment and, accordingly, the identification/description is indefinite. In the rejection based on prior art that follows, the trademark VERILOG is interpreted as implying certain technical features consistent with the

usage in the disclosure of the LoCicero reference and applicant's specification. This interpretation is applied in order to assign an ascertainable scope to the claims and is not intended to suggest that VERILOG is itself the generic terminology for any so-labeled goods and services employing these technical features.

Claim Rejections - 35 USC § 102

6. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

7. Claims 1, 5, 57, and 59 are rejected under 35 U.S.C. 102(b) as being anticipated by Joe LoCicero and Donald E. Thomas, "A Multithreaded Multiple-Language Hardware/Software Cosimulator," 1997, Carnegie Mellon University, Research Report No. CMUCAD-97-34 (hereinafter [LoC1997]).

As per claim 1, [LoC1997] discloses providing a single executable program adapted to create a primary thread and a secondary thread, the primary thread running VERILOG code on a VERILOG simulator, the secondary thread running an interpreter that interprets a scripted routine comprising a user-defined call that is mapped to a VERILOG task (see, for example, section 3 on pp. 6-11, describing the cosimulation environment for Verilog and C++ code; see also the examples on pp. 16-18); providing a user-defined VERILOG function associated with the interpreter (see, for example, section 3 on pp. 6-11; see also the examples on pp. 16-18); upon encountering the user-defined function, passing control from the VERILOG simulator to the interpreter to interpret the scripted routine (see, for example, pp. 7-8; see also the examples on pp. 16-18); and upon encountering the user-defined call, passing control from the interpreter to the VERILOG simulator (see, for example, pp. 7-8; see also the examples on pp. 16-18).

As per claim 5, [LoC1997] further discloses synchronizing the VERILOG simulator and the interpreter via semaphores (see, for example, pp. 7-8; event-driven routines to conditionally suspend execution are provided as Verilog constructs and also in the user's C++ code, providing synchronization).

As per claim 57, [LoC1997] further discloses directly sharing variables between the VERILOG simulator and the scripted routines (see, for example, p. 7, paragraph 2, continuing onto p. 8).

As per claim 59, [LoC1997] discloses providing a single executable program adapted to create a primary thread and one or more secondary threads, the primary thread running VERILOG code on a VERILOG simulator, the secondary threads running an interpreter that interprets a scripted routine comprising a user-defined call that is mapped to a VERILOG task (see, for example, section 3 on pp. 6-11, describing the cosimulation environment for Verilog and C++ code, where each segment of C++, encapsulated C, or converted Verilog that constitutes a coroutine is allocated a separate thread; see also the examples on pp. 16-18); providing a plurality of user-defined VERILOG functions associated with a corresponding interpreter (see, for example, section 3 on pp. 6-11; see also the examples on pp. 16-18); upon encountering the user-defined function, passing control from the VERILOG simulator to the interpreter to interpret the scripted routine (see, for example, pp. 7-8; see also the examples on pp. 16-18); and upon encountering the user-defined call, passing control from the interpreter to the VERILOG simulator (see, for example, pp. 7-8; see also the examples on pp. 16-18).

Conclusion

8. All claims are drawn to the same invention claimed in the application prior to the entry of the submission under 37 CFR 1.114 and could have been finally rejected on the grounds and art of record in the next Office action if they had been entered in the application prior to entry under 37 CFR 1.114. Accordingly, **THIS ACTION IS MADE FINAL** even though it is a first action after the filing of a request for continued examination and the submission under 37 CFR 1.114. See MPEP § 706.07(b). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

9. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Eric B. Kiss whose telephone number is (571) 272-3699. The Examiner can normally be reached on Tue. - Fri., 7:00 am - 4:30 pm. The Examiner can also be reached on alternate Mondays.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Tuan Dam, can be reached on (571) 272-3695. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Any inquiry of a general nature should be directed to the TC 2100 Group receptionist: 571-272-2100.

Eric B. Kiss
May 25, 2007